ABSTRACT

An architecture for creating multiple operating voltage MOSFETs. Generally, an integrated circuit structure includes a semiconductor area with a major surface formed along a plane and first and second spaced-apart doped regions formed in the surface. A third doped region forming a channel of different conductivity type than the first region is positioned over the first region. A fourth doped region of a different conductivity and forming a channel is positioned over the second region. The process of creating the gate structure for each of the two transistors allows for the formation of oxide layers of different thickness between the two transistors. The transistors are therefore capable of operating at different operating voltages (including different threshold voltages). Each transistor further includes fifth and sixth layers positioned respectively over the third and fourth regions and having an opposite conductivity type with respect to the third and fourth regions.

In an associated method of manufacturing the semiconductor device, a first and second source/drain regions are formed in a semiconductor layer. A first field-effect transistor gate region, including a channel and a gate electrode is formed over the first source drain region and a second field-effect transistor gate region is formed over the second source/drain region. Fifth and sixth source/drain regions are then formed for each of the first and second field-effect transistors and further having the appropriate conductivity type. Variable thickness gate oxides are created by appropriately masking, etching, and regrowing gate oxides. As a result, the formed transistors operate at different operating voltages. Thus a plurality of such transistors operating at different operating voltage (as a function of the gate oxide thickness) can be formed in an integrated circuit.